VINAYAKA MISSIONS UNIVERSITY, SALEM

TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- VLSI DESIGN

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2012 REGULATION

I SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Applied Mathematics for Electronics Engineers	MATHS	3	1	0	4
2	Advanced Digital System Design	ECE	3	0	0	3
3	VLSI Design Technology	ECE	3	1	0	4
TOTAL						**11**

II SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	ASIC Design	ECE	3	0	0	3
2	Solid State Device Modelling and Simulation	ECE	3	1	0	4
3	Elective I	ECE	3	0	0	3
PRACTICAL						
4	VLSI Design Lab I	ECE	0	0	2	2
TOTAL						**12**

III SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Analysis and Design of Analog Integrated Circuits	ECE	3	0	0	3
2	Computer Aided Design of VLSI Circuits	ECE	3	1	0	4
3	Computer Architecture and Parallel Processing	CSE	3	0	0	3
TOTAL						**10**

IV SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Embedded Systems	ECE	3	0	0	3
2	Elective II	ECE	3	0	0	3
3	Elective III	ECE	3	0	0	3
PRACTICAL						
4	VLSI Design Lab II	ECE	0	0	2	2
TOTAL						**11**

V SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Elective IV	ECE	3	0	0	3
2	Elective V	ECE	3	0	0	3
3	Elective VI	ECE	3	0	0	3
PRACTICAL						
4	Project Work Phase I	ECE	0	0	6	6
TOTAL						**15**

VI SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
PRACTICAL						
1	Project Work Phase II	ECE	0	0	12	12
TOTAL						**12**

Overall Credits

S.No	Semester	Credits
1	I	11
2	II	12
3	III	10
4	IV	11
5	V	15
6	V1	12
Total		**71**

ELECTIVES LIST

S.No.	Course Title	Offering Department	L	T	P	C
1	Digital Control Engineering	EEE	3	0	0	3
2	Low Power VLSI Design	ECE	3	0	0	3
3	VLSI Signal Processing	ECE	3	0	0	3
4	CMOS VLSI Design	ECE	3	0	0	3
5	Analog VLSI Design	ECE	3	0	0	3
6	Testing of VLSI Circuits	ECE	3	0	0	3
7	VLSI Architecture & Design Methodologies	ECE	3	0	0	3
8	Advanced Digital Image Processing	ECE	3	0	0	3
9	Reliability Engineering for Electronics	ECE	3	0	0	3
10	Electromagnetic Interference and Compatibility	ECE	3	0	0	3
11	Advanced Digital Signal Processing	ECE	3	0	0	3
12	Real Time Operating Systems	ECE	3	0	0	3
13	Software Technology for Embedded System	ECE	3	0	0	3
14	MEMS	ECE	3	0	0	3
15	Mobile Computing	ECE	3	0	0	3
16	Data Communication & Networks	ECE	3	0	0	3
17	DSP Processors	ECE	3	0	0	3
18	Soft Computing Techniques	CSE	3	0	0	3
19	Advanced Robotics & Automation	ECE	3	0	0	3
20	Fuzzy Logic & Artificial Intelligence	CSE	3	0	0	3
21	Video Processing	ECE	3	0	0	3
22	Cyber Security	CSE	3	0	0	3

	Semester I	L	T	P	C
	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	**3**	**1**	**0**	**4**

(Common to Applied Electronics and Embedded System Technology)

AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

To make the student learn to apply mathematics in their field with the advanced topics as fuzzy logic, dynamic programming etc...

UNIT I: FUZZY LOGIC **9**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY **9**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES **9**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING **9**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V: QUEUEING MODELS **9**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.

2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).

	Semester I	L	T	P	C
	ADVANCED DIGITAL SYSTEM DESIGN	**3**	**0**	**0**	**3**

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA **9**

Shannon's expansion theorem, Conseusus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC **9**

Linear seperability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS **9**

Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS **9**

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:

1. William I. Fletcher, “An Engineering Approach to Digital Design" , Prentice Hall of India, 1996.
2. James E. Palmer, David E. Perlman, “Introduction to Digital Systems", Tata McGraw Hill, 1996.
3. N.N. Biswas, "Logic Design Theory", Prentice Hall of India, 1993.
4. S. Devadas, A. Ghosh and K. Keutzer, "Logic Synthesis", Mc Graw Hill, 1994.

	Semester I	L	T	P	C
	VLSI DESIGN TECHNOLOGY	**3**	**1**	**0**	**4**

AIM:

- The aim of this course is to describe the design, technology and manufacture of MOS integrated circuits and future nanoscale electron devices.
- It will provide a firm foundation for those wishing to pursue careers in applications or in research/development in the field of semiconductor devices/circuits.

OBJECTIVES:

On completion of the module students should have developed an awareness of the requirements for IC technology. Understand how device miniaturization has led to improved device performance and the potential limits to this process.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES. 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN. 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

TEXT BOOK:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. Doughlas A.Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.

REFERENCES

1. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
2. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
3. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
4. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
5. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education.2002.

	Semester II	L	T	P	C
	ASIC DESIGN	**3**	**0**	**0**	**3**

AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENTAND 9 ROUTING

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS

REFERENCES:

1. M.J.S .Smith, “Application - Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays” Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	Semester II	L	T	P	C
	SOLID STATE DEVICE MODELING AND SIMULATION	**3**	**1**	**0**	**4**

AIM:

This course deals with fundamentals of electronics involved in the design of VLSI circuits.

OBJECTIVES:

At the end of the course, students should be able to understand

- CMOS processing technology and Basic CMOS circuits, characteristics and performance.
- Designing of combinational and sequential circuits in CMOS**.**

UNIT I : MOSFET DEVICE PHYSICS 9

MOSFET capacitor, Basic operation, Basic modeling,Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II: NOISE MODELING 9

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III: BSIMV4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.

UNIT IV: OTHER MOSFET MODELS 9

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model)

UNIT V: MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE 9

Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003.
2. Christian C. Enz, Eric A. Vittoz, "Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design", John Wiley & Sons, Ltd, 2006.

	Semester II	L	T	P	C
	VLSI DESIGN LAB I	**0**	**0**	**2**	**2**

LIST OF EXPERIMENTS

1. Design Entry Using VHDL or Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.
5. SPICE simulations for small size standard cells.
6. SPICE simulations for analog circuit modules - Common source amplifier, source follower, cascode amplifiers, Differential amplifiers, Two stage Operational Amplifiers.

TOTAL: 30 HOURS

REFERENCES:

1. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001
2. M.J.S .Smith, "Application - Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "Field Programmable Gate Arrays" Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.

	Semester III	L	T	P	C
	ANALYSIS & DESIGN OF ANALOG INTEGRATED CIRCUITS	**3**	**0**	**0**	**3**

AIM:

The key aim of this module is to provide the background and the methods for the understanding of the operation of basic analogue CMOS cells, and how to design common functions.

OBJECTIVE:

After this course the students can adopts strongly industrial perspective and design methods for manufacturability and robustness as well as cost are given high priority.

UNIT I: MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II: CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current Mirrors - Active loads –Voltage and current references: Supply-insensitive biasing, Temperature-insensitive biasing. Output stages: Emitter follower, Source Follower and Class B Push pull output stages.

UNIT III: OPERATIONAL AMPLIFIERS 9

Applications of operational amplifiers, Deviations from ideality in real operational amplifiers, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV: ANALOG MULTIPLIER AND PLL 9

Precision Rectification- Analog Multipliers employing the bipolar transistor, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits, Noise in Integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Basic Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

TOTAL: 45 HOURS

TEXT BOOK:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.

REFERENCE BOOKSS:

1. Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000
2. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modeling and Technology", Prentice Hall of India Pvt. Ltd., 2004.
3. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons, Inc.,2003.
4. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition- Oxford University Press-2003

	Semester III	L	T	P	C
	COMPUTER AIDED DESIGN OF VLSI CIRCUITS	**3**	**1**	**0**	**4**

AIM:

The aim of this course is to give the students knowledge about the usage of computer for the design of VLSI circuits. It also provides the flow of process involved and how design can be simulated.

OBJECTIVE:

At the end of this course the student will have knowledge in using computer simulation software for designing the VLSI circuits.

UNIT I **9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II **9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III **9**

Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV **9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V **9**

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
3. Drechsler, R., Evolutionary Algorithms for VLSI CAD, Kluwer Academic Publishers, Boston, 1998.

4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, Algorithms and Techniques for VLSI Layout Synthesis, Kluwer Academic Publishers, Boston, 1989.

	Semester III	L	T	P	C
	COMPUTER ARCHITECTURE & PARALLEL PROCESSING	3	0	0	3

AIM:
Any VLSI design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING 9
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.
Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLGIES 9
Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.
Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING 9
Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.
Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES 9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING 9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:
1. Kai Hwang "Advanced Computer Architecture", Tata McGraw Hill International, 2001.

REFERENCE BOOKS:
1.John L. Hennessy, David A. Petterson, "Computer Architecture: A Quantitative Approach", 4th Edition, Elsevier, 2007.
2.Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture – A design Space Approach". Pearson Education,2003.
3.David E. Culler, Jaswinder Pal Singh with Anoop Gupta "Parallel Computer Architecture" ,Elsevier, 2004.
4.John P. Shen. "Modern processor design Fundamentals of super scalar processors", Tata McGraw Hill 2003.
5.Sajjan G. Shiva "Advanced Computer Architecture", Taylor & Francis, 2008.
6.V.Rajaraman, C.Siva Ram Murthy, "Parallel Computers- Architecture and Programming", Prentice Hall India, 2008.

	Semester IV	L	T	P	C
	EMBEDDED SYSTEMS	**3**	**0**	**0**	**3**

AIM:

This subject provides all basic concepts of embedded systems and their implementation in C language.

OBJECTIVE:
To make the student learn, the embedded system implementation in C language.

UNIT I INTRODUCTION **9**
Examples of Embedded Systems, Typical hardware, Terminology, Gates, Timing diagrams, Memory, Microprocessors, buses, direct memory access, interrupts, built-ins on the microprocessor, conventions used on schematics.

UNIT II INTERRUPTS & SOFTWARE ARCHITECTURES **9**
Interrupt basics, shared data problem, interrupt latency; Software architectures – Round Robin, Round Robin with interrupts, function queue scheduling architecture, real time operating system architecture, selecting an architecture.

UNIT III - INTRODUCTION TO REAL TIME OPERATING SYSTEMS AND OPERATING SYSTEM SERVICES **9**
Tasks and task states, Tasks and data, semaphores and shared data, Message queues, Mailboxes and pipes, Timer functions, Events, Memory management, Interrupt routines in an RTOS environment

UNIT IV EMBEDDED SOFTWARE DEVELOPMENT AND DEBUGGING TECHNIQUES **9**
The compilation process, native versus cross compilers, Libraries – run time libraries, writing a library, using alternative libraries, using a standard library, Porting kernels, Downloading. Debugging techniques, Emulation techniques,

UNIT V BASIC DESIGN USING A REAL TIME OPERATING SYSTEM & DESIGN EXAMPLES **9**
Principles, Encapsulating semaphores and queues, Hard time scheduling considerations, saving memory space and power.
Embedded system design and coding for an automatic chocolate vending machine, case study of an embedded system for an adaptive cruise control system in a car, case study of an embedded system for a smart card.

TOTAL: 45 HOURS

TEXT BOOKS:
(1) “An Embedded Software Primer”, David E Simon, Pearson Education, 2007
(2) “Embedded Systems Design”, Second Edition, Steve Heath, Elsevier
(3) “Embedded Systems”, Raj Kamal, Tata McGraw Hill Education Private Limited, New Delhi

REFERENCE BOOKS:
(1) Jonartthan W. Valvano Brooks/cole “Embedded Micro computer Systems. Real time Interfacing ", Thomson learning 2001.
(2) Heath, Steve, “Embedded Systems Design ", Newnes 1997.

	Semester IV	L	T	P	C
	VLSI Design Lab II	**0**	**0**	**2**	**2**

1.) Implementation of 8 Bit ALU in FPGA / CPLD.

2.) Implementation of 4 Bit Sliced processor in FPGA / CPLD.

3.) Implementation of Elevator controller using embedded microcontroller.

4.) Implementation of Alarm clock controller using embedded microcontroller.

5.) Implementation of model train controller using embedded microcontroller.

6.) System design using PLL.

	ELECTIVE	L	T	P	C
	DIGITAL CONTROL ENGINEERING	3	0	0	3

AIM:

To enhance the knowledge of student with various algorithms and techniques to apply in controllers.

OBJECTIVE:

- To study the basic digital control system design and its stability testing.
- To study the models of digital devices and systems.
- To learn about digital control algoirithms.
- To study about control systems analysis using state variable methods.
- To analyse the control systems using state variable methods.

Unit I Digital Control, Signal Processing in digital control 9

Control sytem terminology – computer based control – control theory – classical approach to analog controller design – configuration of the basic digital control scheme – Principles of signal conversion – Basic discrete time signals – Time domain models for discrete time sytems –Transfer function models – frequency response – stability on the z-plane and the Jury Stability Criterion – Sample and Hold Systems – sampled spectra and aliasing – reconstruction of analog signals – Choice of sampling rate – Proinciples of discretization

Unit II Models of Digital Control Devices and Systems 9

Z – Domain Description of sampled contineous time Plants – z – domain Description of Systems with Dead–Time – Implementation of Digital Controllers – Tunable PID Controllers – Digital Temperature Control Systems – Digital Position Control Systems – Stepping Motor and Their Control – Programmable Logic Controllers.

Unit III Design of digital Control Algorithms 9

Z – Plane Specifications of control Systems Design – Digital Compensator Desingn using Frequency Response Plots – Digital Compensator Desingn using Root Locus Plots – z – Plane Synthesis.

Unit IV Control System analysis using state Variable Methods 9

Vectors and Matrices – State Variable Representations – Conversion of State Variable Models to Transfer Function – Conversion of Transfer Functions to Cononical State Variable Models – Eigen Values and Eigenvectors – State Equations – Controllability and Observability – Equivalence between Transfer Function and State Variable Representation – Multivariable Sytems.

Unit V Practical Aspects of Digital Control Algorithms 9

Mechanisation of control Algorithms using Microprocessors – Microprocessor Based Temperature Control Systems–Case Study – Stepping Motors and their Interfacing to Microprocessors

TOTAL HOURS: 45

Text Books

1. M. Gopal, “Digital Control and State Variable Methods Conventional Intelligent Control Systems”, Tata McGraw Hill, 3rd Edition.
2. M. Gopal, “Digital Control Engineering” New Age International Publishers.

Reference Books:

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995
2. B. C. Kuo, “Digital Control Systems”, Oxford University Press, 2004.

	ELECTIVE	L	T	P	C
	LOW POWER VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

OBJECTIVE:

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I **9**

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II **9**

Circuit -Logic - Special Techniques - Architecture and Systems.

UNIT III **9**

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.

UNIT IV **9**

Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits.

UNIT V **9**

Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques - Software Design for Low Power.

TOTAL HOURS: 45

REFERENCES:

1. Gary Yeap “Practical Low Power Digital VLSI Design", 1997.
2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", 2000.

	ELECTIVE	L	T	P	C
	VLSI SIGNAL PROCESSING	**3**	**0**	**0**	**3**

AIM:

To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low

power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL HOURS: 45

REFERENCES:

1. Keshab K.Parhi, " VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, 'Practical Low Power Digital VLSI Design,' Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	CMOS VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

Analog circuits are essential in interfacing and in building amplifiers and low pass filters. This course introduces design methods for CMOS analog circuit design and implementation of standard MOS integrated circuits and be able to assess their performance taking into account the effects of real circuit parameters.

OBJECTIVE:

At the end of this course the student will be learning, CMOS analog circuits design and simulation using SPICE.

UNIT I - MOS TRANSISTOR THEORY 9

Introduction to I.C Technology. Basic MOS transistors. Threshold Voltage. Body effect. Basic D.C. Equations. Second order effects. MOS models. Small signal A.C characteristics. The complementary CMOS inverter. DC characteristics. Static Load MOS inverters. The differential inverters. Transmission gate.

UNIT II - CMOS PROCESSING TECHNOLOGY 9

Silicon semiconductor technology. Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology. nwell, pwell process. Silicon on insulator. CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latchup.

UNIT II - CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION 9

Resistance estimation. Capacitance estimation. MOS capacitor characteristics. Device capacitances. Diffusion capacitance. SPICE modeling of MOS capacitance. Routing capacitance. Distributed RC effects. Inductance. Switching characteristics. Rise time. Fall time. Delay time. Empirical delay models. Gate delays. CMOS gate transistor sizing. Power dissipation. Scaling of MOS transistor dimensions.

UNIT IV - CMOS CIRCUIT AND LOGIC DESIGN 9

Cmos Logic gate design. Fan in and fan out. Typical CMOS NAND and NOR delays. Transistor sizing. CMOS logic structures. Complementary logic. BICMOS logic. Pseudo nMOS logic. Dynamic CMOS logic. Clocked CMOS logic. Pass transistor logic. CMOS domino logic. NP domino logic. Cascade voltage switch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures.

UNIT V - CMOS SUBSYSTEM DESIGN 9

Data path operations. Addition/subtraction. Parity generators. Comparators. Zero/one detectors. Binary Counters. ALUs. Multiplication. Array, Radix-n, Wallace Tree and Serial Multiplication. Shifters. Memory elements. RWM, Rom, Content Addressable Memory. Control: FSM, PLA Control Implementation.

Total Hours: 45

REFERENCES

1. Neil.H.E. Weste and K.Eshragian, "Principles of CMOS VLSI Design". 2nd Edition. Addison-Wesley , 2000.
2. Douglas a. Pucknell and K.Eshragian., "Basic VLSI Design" 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., "CMOS Circuit Design", 3rd Indian reprint, PHI, 2000.

	ELECTIVE	L	T	P	C
	ANALOG VLSI DESIGN	3	0	0	3

AIM:

This course is intended to introduce the student to learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

OBJECTIVE:

By the end of the term, students should be able to:

- Demonstrate an understanding of MOS terminal characteristics and capacitive effects.
- Create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGESIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor-Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched -Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks -Floating -Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation -Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter-Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit igma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation -Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test uses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT

9

Review of Statistical Concepts -Statistical Device Modeling-Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 HOURS

REFERENCES:

1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May,"Analog VLSI Design -NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	TESTING OF VLSI CIRCUITS	**3**	**0**	**0**	**3**

AIM:

Testing VLSI is essential as these circuits are complex. Hence this paper deals with fundamental techniques used for logic testing.

OBJECTIVE:

At the end of the course the student will be having knowledge on digital testing as applied to VLSI design.

UNIT I BASICS OF TESTING AND FAULT MODELLING **9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS **9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY **9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS **9**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS **9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

Total Hours: 45

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

	ELECTIVE	L	T	P	C
	VLSI ARCHITECTURE & DESIGN METHODOLOGIES	**3**	**0**	**0**	**3**

AIM:

This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:

- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

1. INTRODUCTION **9**

Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon's expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

2. ANALOG VLSI AND HIGH SPEED VLSI **9**

Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

3. PROGRAMMABLE ASICS **9**

Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

4. PROGRAMMABLE ASIC DESIGN SOFTWARE **9**

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 - Altera MAX 9000 - Design systems – Logic synthesis – Half gate ASIC – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation

5. LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TOTAL HOURS: 45

REFERENCES:

1. William I. Fletcher “An Engineering approach to Digital Design” Prentice Hall of India 1996
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986
3. M.J.S Smith “Application – specific integrates circuits”, Addison Wesley Longman Inc.1997
4. Frederick J. Hill and Gerald R. Peterson, “Computer Aided Logical Design with emphasison VLSI”.

	ELECTIVE	L	T	P	C
	ADVANCED DIGITAL IMAGE PROCESSING	3	0	0	3

AIM:

This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGE TRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION 9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION 9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding,

Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression

UNIT IV: COLOUR IMAGE PROCESSING 9

Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quatization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING 9

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation,Basic Morphological Algorithms,Extension to Gray scale Images.

TOTAL: 45 HOURS

REFERENCE BOOKS:

1) S.Jayaraman, S.Esakkirajan and T.VeeraKumar, "Digital Image processing, Tata Mc Graw Hill publishers, 2009

2) Gonzalez, R.E.Woods, "Digital Image Processing", 3rd Edition, Pearson Education, India, 2009.

3) John W.Woods, "Multidimensional Signal, Image and Video Processing and Coding" Elsevier Academic Press Publications 2006, ISBN-13: 978-0-12– 088516-9.

	ELECTIVE	L	T	P	C
	RELIABILITY ENGINEERING FOR ELECTRONICS	**3**	**0**	**0**	**3**

AIM:

This course aims to provide the student to apply engineering knowledge and specialist techniques to prevent or to reduce the likelihood or frequency of failures.

OBJECTIVE:

The students will be able to understand the ways in which product fail, the effects of failure and aspects of design, manufacture, maintenance and use which affect the likelihood of failure.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliablity of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design, software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT 9

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for
reliability.

TOTAL HOURS: 45

REFERENCES:

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, "Practical Reliability Engineering", 4th edition, John Wiley & Sons, 2002

2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, “AT & T Reliability Manual”, 5th Edition, New
York, 1998
3. Gregg K. Hobbs, “Accelerated Reliability Engineering - HALT and HASS”, John Wiley & Sons, New York, 2000.
4. Lewis, “Introduction to Reliability Engineering”, 2nd Edition, Wiley International, 1996.

	ELECTIVE	L	T	P	C
	ELECTROMAGNETIC INTERFERENCE & COMPATIBILITY	**3**	**0**	**0**	**3**

AIM:

To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

OBJECTIVES:

- To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.
- To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

UNIT I EMI/EMC CONCEPTS **9**

EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES **9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES **9**

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS **9**

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS **9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL HOURS: 45

REFERENCES:

1.V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2.Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3.Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.
4.C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992.
5.Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

	ELECTIVE	L	T	P	C
	ADVANCED DIGITAL SIGNAL PROCESSING	**3**	**0**	**0**	**3**

AIM:

Students will be introduced in actual advanced issues related to signal processing, mainly using time-frequency signal analysis.

OBJECTIVE:

The goal of advanced digital signal processing course is to provide a comprehensive coverage of signal processing methods and tools, including leading algorithms for various applications.

1. DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes, Expectations, Variance, Co -Variance, Scalar Product, Energy of Discrete Signals - Parseval's Theorem, Wiener Khintchine Relation- Power Spectral Density- Periodogram -Sample Autocorrelation- Sum Decomposition Theorem, Spectral Factorization Theorem - Discrete Random Signal Processing by Linear Systems - Simulation of White Noise - Low Pass Filtering of White Noise.

2. SPECTRUM ESTIMATION 9

Non-Parametric Methods-Correlation Method - Co-Variance Estimator- Performance Analysis of Estimators - Unbiased, Consistent Estimators-Periodogram Estimator-Barlett Spectrum Estimation-Welch Estimation- Model based Approach - AR, MA, ARMA Signal Modeling-Parameter Estimation using Yule-Walker Method

3. LINEAR ESTIMATION AND PREDICTION 9

Maximum likelihood criterion-efficiency of estimator-Least mean squared error criterion - Wiener filter- Discrete Wiener Hoff equations-Recursive estimators-Kalman filter-Linear prediction, prediction error- whitening filter, inverse filter-Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Toeplitz system of equations.

4. ADPATIVE FILTERS 9

FIR adaptive filters-Newton's steepest descent method -adaptive filter based on steepest descent method- Widrow Hoff LMS adaptive algorithm- Adaptive channel equalization-Adaptive echo chancellor-Adaptive noise cancellation-RLS adaptive filters-Exponentially weighted RLS-sliding window RLS-Simplified IIR LMS adaptive filter.

5. MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate - Interpolation and Decimation - continuous time model - Direct digital domain approach - Decimation by an integer factor - Interpolation by an integer factor - Single and multistage realization - poly phase realization - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

TOTAL: 45 HOURS

Text Books:

1. Monson H.Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc., New York, 1996.

References:

1. Sopocles J.Orfanidis, Optimum Signal Processing, McGraw Hill, 1990.
2. John G.Proakis, Dimitris G.Manolakis, Digital Signal Processing Prentice Hall of India, 1995.

	ELECTIVE	L	T	P	C
	REAL TIME OPERATING SYSTEMS	**3**	**0**	**0**	**3**

AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:

To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS **9**

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling.

UNIT II: OVERVIEW OF RTOS **9**

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES **9**

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL **9**

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V: RTOS APPLICATION DOMAINS **9**

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

TOTAL HOURS: 45

REFERENCES:

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.

2. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.

3 Charles Crowley, “Operating Systems-A Design Oriented approach” McGraw Hill 1997.

4 C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.

5. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999.

6. Mukesh Sighal and N G Shi “Advanced Concepts in Operating System”, McGraw Hill 2000.

	ELECTIVE	L	T	P	C
	SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS	3	0	0	3

AIM:

To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

OBJECTIVE:

- To study basic programming concepts
- To learn the C and assembly.
- To learn about object oriented analysis and design.
- To learn about UML and its architectures.

1. LOW LEVEL PROGRAMMING IN C **9**

Primitive data types – Functions – recursive functions – Pointers - Structures – Unions – Dynamic memory allocations – File handling – Linked lists

2. C AND ASSEMBLY **9**

Programming in Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

3. OBJECT-ORIENTED ANALYSIS AND DESIGN **9**

Connecting the Object Model with the Use Case Model. Key Strategies for Object-Identification - Underline the Noun Strategy. Identify the Casual Objects - Identify Services (Passive Contributors) - Identify Real-World Items - Identify Physical Devices - Identify Key Concepts - Identify Transactions - Identify Persistent Information - Identify Visual Elements. Identify Control Elements - Apply Scenarios.

4. UNIFIED MODELLING LANGUAGE **9**

Object State Behaviour - UML State charts - Role of Scenarios in the Definition of Behaviour - Timing Diagrams - Sequence Diagrams - Event Hierarchies - Types and Strategies of Operations - Architectural Design in UML Concurrency Design - Representing Tasks - System Task Diagram - Concurrent State Diagrams - Threads. Mechanistic Design - Simple Patterns.

5. CASE STUDIES **9**

Multi-threaded applications – assembling embedded applications – polled waiting loop and interrupt driven I/O – preemptive kernels and shared resources - system timer – scheduling – client server computing.

TOTAL HOURS: 45

REFERENCES:

1. Bruce Powel Douglas, “Real-Time UML, Second Edition: Developing Efficient Objects for Embedded Systems (The Addison-Wesley Object Technology Series)”, 2 edition (October 29, 1999), Addison-Wesley.
2. 2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.

3. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet” PHI 2002.

	ELECTIVE	L	T	P	C
	MEMS	**3**	**0**	**0**	**3**

AIM:

This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:

At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I MEMS AND MICROSYSTEMS 9

Typical MEMs and Microsystems, materials for MEMS - active substrate materials- Silicon and its compounds, Silicon piezoresistors, Gallium Arsenide, quartz, polymers. Micromachining-photolithography, thin film deposition, doping, etching, bulk machining, wafer bonding, LIGA

UNIT II MICROSENSORS AND ACUATORS 9

Mechanical sensors and actuators – beam and cantilever, piezoelectric materials, thermal sensors and actuators- micromachined thermocouple probe, Peltier effect heat pumps, thermal flow sensors, Magnetic sensors and actuators- Magnetic Materials for MEMS, Devices

UNIT III MICRO OPTO ELECTRO MECHANICAL SYSTEMS 9

Fundamental principle of MOEMS technology, light modulators, beam splitter, microlens, digital micromirror devices, light detectors, optical switch

UNIT IV MICROFLUIDIC SYSTEMS 9

Microscale fluid, expression for liquid flow in a channel, fluid actuation methods, dielectrophoresis, microfluid dispenser, microneedle, micropumps-continuous flow system

UNIT V APPLICATIONS OF MEMS 9

Drug delivery, micro total analysis systems (MicroTAS) detection and measurement methods, microsystem approaches to polymerase chain reaction (PCR), DNA hybridization, Electronic nose, Bio chip

TOTAL HOURS: 45

REFERENCE BOOK:

1. Tai Ran Hsu , " MEMS and Microsystems design and manufacture", Tata McGraw Hill Publishing Company, New Delhi, 2002
2. NitaigourPremchandMahalik, " MEMS", Tata McGraw Hill Publishing Company, New Delhi, 2007

3. Wanjun Wang, Steven A.Soper " BioMEMS- Technologies and applications", CRC Press,Boca Raton,2007.
4. Abraham P. Lee and James L. Lee, BioMEMS and Biomedical Nano Technology, Volume I, Springer 2006.

	ELECTIVE	L	T	P	C
	MOBILE COMPUTING	**3**	**0**	**0**	**3**

AIM:

The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:

At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT – I: WIRELESS TRANSMISSION **9**

Frequency for radio transmission- signals- antennas- signal propagation- multiplexing- modulation- spread spectrum- medium axis control- SDMA- FDMA- TDMA- CDMA- comparisons.

UNIT – II: TELECOMMUNICATION SYSTEM **9**

GSM- DECT- Tetra- UMTS- IMT 2000- GPRS

UNIT – III: WIRELESS LAN **9**

Introduction - Network Taxonomy -IEEE 802.11 standard- hyper LAN - Adhoc network- Bluetooth.

UNIT – IV: MOBILE NETWORK LAYER **9**

Mobile IP- Dynamic post configuration protocol- mobile Adhoc network- DSDV- DSR- AODV- ZRP- OVMR.

UNIT – V: MOBILE TRANSPORT LAYER AND APPLICATION **9**

TCP- WAP- Architecture- WDGP- WTLS- WTP- WSP- WML- WAE- WML script- WTA.

TOTAL HOURS:45

TEXT BOOK

1. Jochen Schiller, “Mobile Communications”, Second Edition, Prentice Hall Of India/Pearson Education, 2005.

REFERENCE

1. WILLIAM STALLINGS**, “**Wireless Communications and Networks”, Second Edition, Prentice Hall Of India/Pearson Education 2004.

	ELECTIVE	L	T	P	C
	DATA COMMUNICATION AND NETWORKS	**3**	**0**	**0**	**3**

AIM:

To learn all parts of communication software in layered architecture.

OBJECTIVE:

- To study the basics on computer networks and its protocols
- To study the transport layer protocol of OSI model.
- To learn about network layer of OSI model.
- To study data link and MAC layer of OSI model.
- To learn about network security in computer networks.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS 9

An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS 9

Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER 9

Datagram and virtual circuit service - Routing principles - Internet protocols IPVI Addressing and routing datagram format _ IP fragmentation and reassembly - ICMP routing in the internet - Router - Input ports - Switching fabrics - Output ports - Queuing - IPV6 packet format transition from IPV4 to IPV6 Multicast routing.

UNIT IV DATA LINK AND MAC LAYER 9

Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM-X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA 9

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL HOURS: 45

REFERENCE BOOKS:

1. K.Kurose and K.W.Ross - "Computer network" Addison Wesley.(1997)
2. A.S . Tanenbaum "Computer Networks "- (3/e), (2001).
3. T.N.Saadavi,M.H.Ammar & AL . Halleem" Fundamentals of Telecommunication Networks " - Wiley J.K.Buford - "Multimedia Systems" - Addison Wesley.(2001)

	ELECTIVE	L	T	P	C
	DSP PROCESSORS	**3**	**0**	**0**	**3**

AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S **9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP's – Multiple access memory – Multi – port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP's – On Chip Peripherals.

UNIT II: TMS320C5X PROCESSOR **9**

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR **9**

Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV: ADSP PROCESSORS **9**

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS **9**

Architecture of TMS320C54X: Pipe line operation, Code Composer Studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 HOURS

TEXT BOOK:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" - Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008.

REFERENCE BOOKS:

1. User guides Texas Instrumentation, Analog Devices, Motorola.
2. Simon Haykin “Adaptive filter theory”, Prentice Hall, 2001.
3. Anil K Jain “Fundamental of Digtal image processing”, Prentice Hall, 1989.

	ELECTIVE	L	T	P	C
	SOFT COMPUTING TECHNIQUES	3	0	0	3

AIM:

This course will provide a comprehensive and structured exposure to Soft Computing Techniques i.e Artificial Neural Networks, Fuzzy Logic, Genetic Algorithm, Particle Swarm Optimization.

OBJECTIVE:

To make the student learn, all types of soft computing techniques and how it is applied in various fields.

1. INTRODUCTION **9**

Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

2. ARTIFICIAL NEURAL NETWORKS **9**

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

3. FUZZY LOGIC SYSTEM **9**

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

4. GENETIC ALGORITHM **9**

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and anD-colony search techniques for solving optimization problems.

5. APPLICATIONS **9**

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox.
Stability analysis of Neural-Network interconnection systems. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

TOTAL: 45 HOURS

REFERENCES:

1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing House, 1999.
2. KOSKO,B. "Neural Networks And Fuzzy Systems", Prentice-Hall of India Pvt. Ltd., 1994.
3. KLIR G.J. & FOLGER T.A. "Fuzzy sets, uncertainty and Information", Prentice-Hall of India Pvt. Ltd., 1993.
4. Zimmerman H.J. "Fuzzy set theory-and its Applications"-Kluwer Academic Publishers, 1994.
5. Driankov, Hellendroon, "Introduction to Fuzzy Control", Narosa Publishers.

	ELECTIVE	L	T	P	C
	ADVANCED ROBOTICS & AUTOMATION	**3**	**0**	**0**	**3**

AIM:

The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:

At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION **9**

Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS **9**

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS **9**

Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATONS **9**

Material Transfer & Machine Loading / Unloading General Consideration in robot material handling transfer applications – Machine loading and unloading. Processing Operations Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V ASSEMBLY AND INSPECTION **9**

Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL HOURS: 45

REFERENCES:

1. Fu, Gonazlez.K.S., R.C. and Lee, C.S.G., Robotics (Control, Sensing, Vision and Intelligence), McGraw Hill, 1968
2. Wesley.E, Snyder.R, Industrial Robots, "Computer Interfacing and Control", Prentice Hall International Edition, 1988
3. Asada and Slotine, "Robot analysis and Control", John Wiley and sons, 1986
4. Philippe Coiffet, "Robot technology" - Vol.II (Modelling and Control), Prentice Hall Inc., 1983
5. Groover.M.P., Mitchell, Weiss, "Industrial Robotics Technology Programming and Applications", Tata McGraw Hill, 1986

	ELECTIVE	L	T	P	C
	FUZZY LOGIC & ARTIFICIAL INTELLIGENCE	**3**	**0**	**0**	**3**

AIM:

To provide in depth knowledge to students about the artificial neural networks and also Fuzzy Logic as well as application of it.

OBJECTIVE:

- To make the student learn to improve their skills over artificial neural network and their application.
- To make the student learn to understand the concepts of fuzzy logic and their application.

UNIT I FUNDAMENTALS OF ANN **9**

Introduction – Neuron Physiology – Specification of the brain – Eye neuron model - Fundamentals of ANN –Biological neurons and their artificial models – Learning processes –different learning rules – types of activation functions– training of ANN – Perceptron model (both single & multi-layer) – training algorithm – problems solving using learning rules and algorithms – Linear seperability limitation and its over comings

UNIT II ANN ALGORITHM **9**

Back propagation training algorithm – Counter propagation network – structure & operation – training – applications of BPN & CPN -Statistical method – Boltzmann training – Cauchy training – Hop field network and Boltzmann machine – Travelling sales man problem - BAM – Structure – types – encoding and retrieving – Adaptive resonance theory – Introduction to optical neural network – Cognitron & Neocognitron

UNIT III APPLICATION OF ANN **9**

Hand written and character recognition – Visual Image recognition –- Communication systems – call processing– Switching – Traffic control – routing and scheduling –Articulation Controller - Neural Acceleration Chip (NAC)

UNIT IV INTRODUCTION TO FUZZY LOGIC **9**

Introduction to fuzzy set theory — membership function - basic concepts of fuzzy sets – Operations on fuzzy sets and relations, classical set Vs fuzzy set – properties of fuzzy set – fuzzy logic control principles – fuzzy relations – fuzzy rules – Defuzzification – Time dependent logic – Temporal Fuzzy logic (TFC) – Fuzzy Neural Network (FANN) – Fuzzy logic controller – Fuzzification & defuzzification interface.

UNIT V APPLICATION OF FUZZY LOGIC **9**

Application of fuzzy logic to washing machine – Vaccum cleaner – Water level controller – temperature controller- Adaptive fuzzy systems – Fuzzy filters – Sub band coding – Adaptive fuzzy frequency hopping.

TOTAL HOURS:45

REFERENCE BOOKS:

1. Freeman & Skapura, “Neural Networks”, Addison - Wesley, 1991.
2. Zurada.J.M., “Introduction to Artificial Neural Systems”, West, 1992.
3. Simon Haykin, Macmillan, “Neural Networks”, 1994.
4. Yagnanarayana.B., “Artificial Neural Networks”, Prentice Hall of India, 2006.

	ELECTIVE	L	T	P	C
	VIDE PROCESSING	3	0	0	3

AIM

The purpose of Video Processing course is to cover the fundamentals of digital video signal generation and further processing over the communication systems.

OBJECTIVE

To learn the basic concepts of video processing
To learn about the various methodologies for motion estimation
To learn the basic concepts of coding systems
To understand about the waveform based video coding techniques
To understand about the content dependent and scalable video coding techniques

UNIT I VIDEO FORMATION, PERCEPTION AND REPRESENTATION 9

Color Perception and Specification, Video Capture and Display, Analog Video Raster, Analog Color Television Systems, Digital Video.

UNIT II TWO-DIMENSIONAL MOTION ESTIMATION 9

General Methodologies, Pixel-Based Motion Estimation,, Block Matching Algorithm, Mesh-based Motion estimation, Global Motion Estimation, Region –Based Motion Estimation, Mutiresolution Motion Estimation, Application of Motion Estimation in Video Coding.
Feature-based Motion Estimation.

UNIT III FOUNDATONS OF VIDEO CODING 9

Overview of Coding Systems, Basic Notions in Probability and Information Theory, Information Theory for Source Coding, Binary Encoding, Scalar Quantization , Vector Quantization.

UNIT IV WAVEFORM-BASED VIDEO CODING 9

Block-Based Transform Coding, Predictive Coding, Video Coding Using Temporal Prediction and Transform Coding.

UNIT V CONTENT-DEPENDENT & SCALABLE VIDEO CODING 9

Two-Dimensional Shape Coding, Texture coding for Arbitrarily Shaped Regions, Joint Shape & Texture Coding, Region-Based Video Coding, Object-based Video Coding. Basic Modes of Scalability,Object Based Scalability, Wavelet-transform Based Coding.

TOTAL HOURS: 45

TEXT BOOKS:

1. YaoWang, Jorn Ostermann, Ya-Qin Zhang,"Video Processing & Communication", Pearson Education - India, New Delhi, Prentice Hall, 2002.

REFERENCES:

M. Tekalp, Digital Video Processing, Prentice Hall, 1995.

	ELECTIVE	L	T	P	C
	CYBER SECURITY	**3**	**0**	**0**	**3**

AIM

To produce the knowledge on cyber security essentials

OBJECTIVE

- To study the cyber security fundamentals
- To study the various techniques on attack and exploitation
- To study in detail about malicious code
- To study about defense and analysis techniques

UNIT I CYBER SECURITY FUNDAMENTALS

Network and security concepts – basic cryptography – Symmetric encryption – Public key Encryption – DNS – Firewalls – Virtualization – Radio Frequency Identification – Microsoft Windows security Principles.

UNIT II ATTACKER TECHNIQUES AND MOTIVATIONS

Antiforensics – Tunneling techniques – Fraud Techniques - Threat Infrastructure.

UNIT III EXPLOITATION

Techniques to gain a foot hold – Misdirection, Reconnaissance, and disruption methods.

UNIT IV MALICIOUS CODE

Self Replication Malicious code – Evading Detection and Elevating privileges – Stealing Information and Exploitation.

UNIT V DEFENSE AND ANALYSIS TECHNIQUES

Memory Forensics – Honeypots – Malicious code naming – Automated malicious code analysis systems – Intrusion detection systems – Defense special file investigation tools.

TOTAL HOURS: 45

TEXT BOOK

1. James Graham, Richard Howard and Ryan Olson, "Cyber Security Essentials", CRC Press, Taylor & Francis Group, 2011.

REFERENCE BOOKS

1. By Dan Shoemaker, Ph.D., William Arthur Conklin, Wm Arthur Conklin, "Cybersecurity: The Essential Body of Knowledge**",** Cengage Learning, 2012.
2. Ali Jahangiri, "Live Hacking: The Ultimate Guide to hacking Techniques & Counter measures for Ethical Hackers & IT Security Experts", 2009.