FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- VLSI DESIGN

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2016 REGULATION

ME VLSI R 2015

I SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Applied Mathematics for Electronics Engineers (common to AE, EST, VLSI)	MATHS	3	1	0	4
2	Advanced Digital System Design (common to AE, EST, VLSI)	ECE	3	0	0	3
3	VLSI Design Technology	ECE	3	1	0	4

TOTAL					**11**

II SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	ASIC Design	ECE	3	0	0	3
2	Solid State Device Modelling and Simulation	ECE	3	1	0	4
3	Elective I	ECE	3	0	0	3
PRACTICAL						
4	VLSI Design Lab I	ECE	0	0	2	2
TOTAL						**12**

III SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Analysis and Design of Analog Integrated Circuits (common to AE, VLSI)	ECE	3	0	0	3
2	Computer Aided Design of VLSI Circuits	ECE	3	1	0	4
3	Computer Architecture and Parallel Processing (common to AE, EST, VLSI)	CSE	3	0	0	3
TOTAL						**10**

IV SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Embedded Systems	ECE	3	0	0	3
2	Elective II	ECE	3	0	0	3

3	Elective III	ECE	3	0	0	3
PRACTICAL						
4	VLSI Design Lab II	ECE	0	0	2	2
TOTAL						**11**

V SEMESTER

S.No.	**Course Title**	**Offering Department**	**L**	**T**	**P**	**C**
THEORY						
1	Elective IV	ECE	3	0	0	3
2	Elective V	ECE	3	0	0	3
3	Elective VI	ECE	3	0	0	3
PRACTICAL						
4	Project Work Phase-I & Viva Voce	ECE	0	0	6	6
TOTAL						**15**

VI SEMESTER

S.No.	**Course Title**	**Offering Department**	**L**	**T**	**P**	**C**
PRACTICAL						
1	Project Work Phase-II & Viva Voce	ECE	0	0	12	12
TOTAL						**12**

Overall Credits

S.No	Semester	Credits
1	I	11
2	II	12
3	III	10
4	IV	11
5	V	15
6	V1	12
Total		**71**

ELECTIVES LIST

S.No.	Course Title	Offering Department	L	T	P	C
1	Low Power VLSI Design	ECE	3	0	0	3
2	VLSI for Wireless Communication	ECE	3	0	0	3
3	MEMS	ECE	3	0	0	3
4	Multimedia Compression Techniques	ECE	3	0	0	3
5	Wireless Security	ECE	3	0	0	3
6	Pattern Recognition & Artificial Intelligent Techniques	ECE	3	0	0	3
7	Wavelets & Multi-resolution Processing	ECE	3	0	0	3
8	Intrusion Detection & Prevention Systems	ECE	3	0	0	3
9	System on Chip	ECE	3	0	0	3
10	Electromagnetic Interference & Compatibility in System Design	ECE	3	0	0	3
11	Cognitive Radio Technology	ECE	3	0	0	3
12	Nano Electronics	ECE	3	0	0	3
13	VLSI Signal Processing	ECE	3	0	0	3
14	CMOS VLSI Design	ECE	3	0	0	3
15	Analog VLSI Design	ECE	3	0	0	3
16	Testing of VLSI Circuits	ECE	3	0	0	3
17	VLSI Architecture & Design Methodologies	ECE	3	0	0	3
18	Mobile Computing	ECE	3	0	0	3
19	Data Communication & Networks	ECE	3	0	0	3
20	DSP Processors	ECE	3	0	0	3

	Semester I	L	T	P	C
	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS (common to AE, EST, VLSI)	**3**	**1**	**0**	**4**

AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

- To understand the concepts of fuzzy logic.
- To make the student learn different matrix methods and some of the applications.
- To understand the concepts of random variables.
- To make the student learn dynamic programming and their applications.
- To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC **9**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY **9**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES **9**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING **9**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V: QUEUEING MODELS **9**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of

India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.

3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).

4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).

	Semester I	L	T	P	C
	ADVANCED DIGITAL SYSTEM DESIGN (common to AE, EST, VLSI)	**3**	**0**	**0**	**3**

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA 9

Shannon's expansion theorem, Conseusus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC 9

Linear seperability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS 9

Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS 9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES 9

Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:

1. William I. Fletcher, “An Engineering Approach to Digital Design" , Prentice Hall of India, 1996.
2. James E. Palmer, David E. Perlman, “Introduction to Digital Systems", Tata McGraw Hill, 1996.
3. N.N. Biswas, "Logic Design Theory", Prentice Hall of India, 1993.
4. S. Devadas, A. Ghosh and K. Keutzer, "Logic Synthesis", Mc Graw Hill, 1994.

	Semester I	L	T	P	C
	VLSI DESIGN TECHNOLOGY	**3**	**1**	**0**	**4**

AIM:

- The aim of this course is to describe the design, technology and manufacture of MOS integrated circuits and future nanoscale electron devices.
- It will provide a firm foundation for those wishing to pursue careers in applications or in research/development in the field of semiconductor devices/circuits.

OBJECTIVES:

On completion of the module students should have developed an awareness of the requirements for IC technology. Understand how device miniaturization has led to improved device performance and the potential limits to this process.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES. 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN. 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

TEXT BOOK:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. Doughlas A.Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.

REFERENCES

1. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
2. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
3. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
4. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
5. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education.2002.

	Semester II	L	T	P	C
	ASIC DESIGN	**3**	**0**	**0**	**3**

AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENTAND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS

REFERENCES:

1. M.J.S .Smith, “Application - Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays” Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	Semester II	L	T	P	C
	SOLID STATE DEVICE MODELING AND SIMULATION	**3**	**1**	**0**	**4**

AIM:

This course deals with fundamentals of electronics involved in the design of VLSI circuits.

OBJECTIVES:

At the end of the course, students should be able to understand

- CMOS processing technology and Basic CMOS circuits, characteristics and performance.
- Designing of combinational and sequential circuits in CMOS

UNIT I : MOSFET DEVICE PHYSICS 9

MOSFET capacitor, Basic operation, Basic modeling,Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II: NOISE MODELING 9

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III: BSIMV4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.

UNIT IV: OTHER MOSFET MODELS 9

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model)

UNIT V: MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE 9

Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng , Tor A. Fjeldly and Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2003.
2. Christian C. Enz, Eric A. Vittoz, “Charge-based MOS Transistor Modeling The EKV model for low-power and RF IC design”, John Wiley & Sons, Ltd, 2006.

	Semester II	L	T	P	C
	VLSI DESIGN LAB I	**0**	**0**	**2**	**2**

LIST OF EXPERIMENTS

1. Design Entry Using VHDL or Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.
5. SPICE simulations for small size standard cells.
6. SPICE simulations for analog circuit modules - Common source amplifier, source follower, cascode amplifiers, Differential amplifiers, Two stage Operational Amplifiers.

TOTAL: 30 HOURS

REFERENCES:

1. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001
2. M.J.S .Smith, "Application - Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "Field Programmable Gate Arrays" Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.

	Semester III	L	T	P	C
	ANALYSIS & DESIGN OF ANALOG INTEGRATED CIRCUITS (common to AE, VLSI)	**3**	**0**	**0**	**3**

AIM:

The key aim of this module is to provide the background and the methods for the understanding of the operation of basic analogue CMOS cells, and how to design common functions.

OBJECTIVE:

After this course the students can adopts strongly industrial perspective and design methods for manufacturability and robustness as well as cost are given high priority.

UNIT I: MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II: CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current Mirrors - Active loads –Voltage and current references: Supply-insensitive biasing, Temperature-insensitive biasing. Output stages: Emitter follower, Source Follower and Class B Push pull output stages.

UNIT III: OPERATIONAL AMPLIFIERS 9

Applications of operational amplifiers, Deviations from ideality in real operational amplifiers, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV: ANALOG MULTIPLIER AND PLL 9

Precision Rectification- Analog Multipliers employing the bipolar transistor, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits, Noise in Integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Basic Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

TOTAL: 45 HOURS

TEXT BOOK:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.

REFERENCE BOOKSS:

1. Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000
2. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modeling and Technology", Prentice Hall of India Pvt. Ltd., 2004.
3. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons, Inc.,2003.

4. Phillip E.Allen Douglas R. Holberg, “CMOS Analog Circuit Design”, Second Edition- Oxford University Press-2003

	Semester III	L	T	P	C
	COMPUTER AIDED DESIGN OF VLSI CIRCUITS	**3**	**1**	**0**	**4**

AIM:

The aim of this course is to give the students knowledge about the usage of computer for the design of VLSI circuits. It also provides the flow of process involved and how design can be simulated.

OBJECTIVE:

At the end of this course the student will have knowledge in using computer simulation software for designing the VLSI circuits.

UNIT I

VLSI DESIGN AUTOMATION **9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II

LAYOUT COMPACTION **9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III

FLOORPLANNING AND ROUTING **9**

Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV

MODELING AND SYNTHESIS **9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V

HIGH LEVEL SYNTHESIS AND SCHEDULING **9**

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
3. Drechsler, R., Evolutionary Algorithms for VLSI CAD, Kluwer Academic Publishers, Boston, 1998.
4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, Algorithms and Techniques for VLSI Layout Synthesis, Kluwer Academic Publishers, Boston, 1989.

	Semester III	L	T	P	C
	COMPUTER ARCHITECTURE & PARALLEL PROCESSING (common to AE, EST, VLSI)	**3**	**0**	**0**	**3**

AIM:

Any VLSI design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:

- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING 9

Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.

Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLGIES 9

Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING 9

Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING 9

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

1. Kai Hwang "Advanced Computer Architecture", Tata McGraw Hill International, 2001.

REFERENCE BOOKS:

1.John L. Hennessy, David A. Petterson, "Computer Architecture: A Quantitative Approach", 4th Edition, Elsevier, 2007.

2.Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture – A design Space Approach". Pearson Education,2003.

3.David E. Culler, Jaswinder Pal Singh with Anoop Gupta "Parallel Computer Architecture" ,Elsevier, 2004.

4.John P. Shen. "Modern processor design Fundamentals of super scalar processors", Tata McGraw Hill 2003.

5.Sajjan G. Shiva "Advanced Computer Architecture", Taylor & Francis, 2008.

6.V.Rajaraman, C.Siva Ram Murthy, "Parallel Computers- Architecture and Programming", Prentice Hall India, 2008.

	Semester IV	L	T	P	C
	EMBEDDED SYSTEMS	**3**	**0**	**0**	**3**

AIM:

This subject provides all basic concepts of embedded systems and their implementation in C language.

OBJECTIVE:
To make the student learn, the embedded system implementation in C language.

UNIT I INTRODUCTION **9**
Examples of Embedded Systems, Typical hardware, Terminology, Gates, Timing diagrams, Memory, Microprocessors, buses, direct memory access, interrupts, built-ins on the microprocessor, conventions used on schematics.

UNIT II INTERRUPTS & SOFTWARE ARCHITECTURES **9**
Interrupt basics, shared data problem, interrupt latency; Software architectures – Round Robin, Round Robin with interrupts, function queue scheduling architecture, real time operating system architecture, selecting an architecture.

UNIT III - INTRODUCTION TO REAL TIME OPERATING SYSTEMS AND OPERATING SYSTEM SERVICES **9**
Tasks and task states, Tasks and data, semaphores and shared data, Message queues, Mailboxes and pipes, Timer functions, Events, Memory management, Interrupt routines in an RTOS environment

UNIT IV EMBEDDED SOFTWARE DEVELOPMENT AND DEBUGGING TECHNIQUES **9**
The compilation process, native versus cross compilers, Libraries – run time libraries, writing a library, using alternative libraries, using a standard library, Porting kernels, Downloading. Debugging techniques, Emulation techniques,

UNIT V BASIC DESIGN USING A REAL TIME OPERATING SYSTEM & DESIGN EXAMPLES **9**
Principles, Encapsulating semaphores and queues, Hard time scheduling considerations, saving memory space and power.
Embedded system design and coding for an automatic chocolate vending machine, case study of an embedded system for an adaptive cruise control system in a car, case study of an embedded system for a smart card.

TOTAL: 45 HOURS

TEXT BOOKS:
(1) "An Embedded Software Primer", David E Simon, Pearson Education, 2007
(2) "Embedded Systems Design", Second Edition, Steve Heath, Elsevier
(3) "Embedded Systems", Raj Kamal, Tata McGraw Hill Education Private Limited, New Delhi

REFERENCE BOOKS:
(1) Jonartthan W. Valvano Brooks/cole "Embedded Microcomputer Systems. Real time Interfacing ", Thomson learning 2001.
(2) Heath, Steve, "Embedded Systems Design ", Newnes 1997.

	Semester IV	L	T	P	C
	VLSI Design Lab II	**0**	**0**	**2**	**2**

1.) Implementation of 8 Bit ALU in FPGA / CPLD.

2.) Implementation of 4 Bit Sliced processor in FPGA / CPLD.

3.) Implementation of Elevator controller using embedded microcontroller.

4.) Implementation of Alarm clock controller using embedded microcontroller.

5.) Implementation of model train controller using embedded microcontroller.

6.) System design using PLL.

TOTAL: 30 HOURS

	ELECTIVE	L	T	P	C
	VLSI SIGNAL PROCESSING	**3**	**0**	**0**	**3**

AIM:

To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low

power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL HOURS: 45

REFERENCES:

1. Keshab K.Parhi, " VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, 'Practical Low Power Digital VLSI Design,' Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	LOW POWER VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

OBJECTIVE:

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I

SIMULATION & PROBABILISTIC POWER ANALYSIS **9**

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II
CIRCUIT, LOGIC & SPECIAL TECHNIQUES **9**

Circuit -Logic - Special Techniques - Architecture and Systems.

UNIT III
ADVANCED TECHNIQUES & PHYSICS OF POWER DISSIPATION **9**

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.

UNIT IV
POWER ESTIMATION & SYNTHESIS FOR LOW POWER **9**

Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits.

UNIT V
STATIC RAM & SOFTWARE DESIGN FOR LOW POWER **9**

Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques - Software Design for Low Power.

TOTAL HOURS: 45

REFERENCES:

1. Gary Yeap “Practical Low Power Digital VLSI Design", 1997.
2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", 2000.

	ELECTIVE	L	T	P	C
	VLSI FOR WIRELESS COMMUNICATION	**3**	**0**	**0**	**3**

AIM:

To make the student understand the application of VLSI circuits in wireless communication.

OBJECTIVE:

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of various VLSI circuits for wireless communicationsystems.

UNIT I

COMPONENTS AND DEVICES **9**

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers.

UNIT II

MIXERS **9**

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Low Frequency Case: Analysis of Gilbert Mixer –Distortion – High - Frequency Case – Noise – A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT III

FREQUENCY SYNTHESIZERS **9**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IV

SUB SYSTEMS **9**

Data converters in communications, adaptive Filters, equalizers and transceivers.

UNIT V

IMPLEMENTATIONS **9**

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System.

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice - Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio – Frequency Integrated Circuits', Cambridge University Press, 2003.

4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design - Circuits and Systems”, Kluwer Academic Publishers, 2000.
5. Behzad Razavi, “ Design of Analog CMOS Integrated Circuits” McGraw - Hill, 1999.
6. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 1997.

	ELECTIVE	L	T	P	C
	MEMS	**3**	**0**	**0**	**3**

AIM:

This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:

At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I MEMS AND MICROSYSTEMS 9

Typical MEMs and Microsystems, materials for MEMS - active substrate materials- Silicon and its compounds, Silicon piezoresistors, Gallium Arsenide, quartz, polymers. Micromachining- photolithography, thin film deposition, doping, etching, bulk machining, wafer bonding, LIGA

UNIT II MICROSENSORS AND ACUATORS 9

Mechanical sensors and actuators – beam and cantilever, piezoelectric materials, thermal sensors and actuators- micromachined thermocouple probe, Peltier effect heat pumps, thermal flow sensors, Magnetic sensors and actuators- Magnetic Materials for MEMS, Devices

UNIT III MICRO OPTO ELECTRO MECHANICAL SYSTEMS 9

Fundamental principle of MOEMS technology, light modulators, beam splitter, microlens, digital micromirror devices, light detectors, optical switch

UNIT IV MICROFLUIDIC SYSTEMS 9

Microscale fluid, expression for liquid flow in a channel, fluid actuation methods, dielectrophoresis, microfluid dispenser, microneedle, micropumps-continuous flow system

UNIT V APPLICATIONS OF MEMS 9

Drug delivery, micro total analysis systems (MicroTAS) detection and measurement methods, microsystem approaches to polymerase chain reaction (PCR), DNA hybridization, Electronic nose, Bio chip

TOTAL HOURS: 45

REFERENCE BOOK:

1. Tai Ran Hsu , " MEMS and Microsystems design and manufacture", Tata McGraw Hill Publishing Company, New Delhi, 2002
2. NitaigourPremchandMahalik, " MEMS", Tata McGraw Hill Publishing Company, New Delhi, 2007
3. Wanjun Wang, Steven A.Soper " BioMEMS- Technologies and applications", CRC Press,Boca Raton,2007.
4. Abraham P. Lee and James L. Lee, BioMEMS and Biomedical Nano Technology, Volume I, Springer 2006.

	ELECTIVE	L	T	P	C
	MULTIMEDIA COMPRESSION TECHNIQUES	**3**	**0**	**0**	**3**

AIM:

To understand and integrate new knowledge within the field.

OBJECTIVE:

- To explore the special features and representations of different data types.
- To analyze different compression techniques for text data and audio signals.
- To analyze various compression techniques for image and video signals.

Unit I – Introduction **9 Hours**

Special features of Multimedia – Graphics and Image Data Representations – Fundamental Concepts in Text, Images, Graphics, Video and Digital Audio – Storage requirements for multimedia applications - Need for Compression – Lossy & Lossless compression techniques – Overview of source coding, Information theory & source models- Kraft McMillan Inequality – vector quantization –LBZ algorithm.

Unit II – Text Compression **9 Hours**

Compression techniques – Huffmann coding – Adaptive Huffmann Coding – Arithmetic coding – Shannon- Fano coding – Dictionary techniques –LZ77, LZ78, LZW family algorithms.

Unit III – Audio Compression **9 Hours**

Audio compression techniques - μ- Law and A- Law compounding - Frequency domain and filtering – Basic sub-band coding –DPC M- ADPCM-DM-LPC-CELP -Application to speech coding – G.722 – Application to audio coding – MPEG audio, progressive encoding for audio – Silence compression techniques.

Unit IV – Image Compression **9 Hours**

MMR coding –Transform Coding – JPEG Standard – Sub-band coding algorithms - Design of Filter banks – Wavelet based compression - Implementation using filters – EZW, SPIHT coders – JPEG 2000 standards - JBIG, JBIG2 standards- Run length coding.

Unit V – Video Compression **9 Hours**

Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II - MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – DVI real time compression – Packet Video.

REFERENCES:

1. Khalid Sayood, *Introduction to Data Compression*, Morgan Kauffman Harcourt India, 2005.
2. David Salomon, *Data Compression – The Complete Reference*, Springer Verlang, 2006.
3. Yun Q.Shi and Huifang Sun, *Image and Video Compression for Multimedia Engineering – Fundamentals, Algorithms & Standards*, CRC press, 2003.
4. Peter Symes, *Digital Video Compression*, McGraw Hill Publication, 2004.
5. Mark Nelson, *Data Compression*, BPB Publishers, 2000.
6. Mark S.Drew and Ze-Nian Li, *Fundamentals of Multimedia*, PHI, 2003

	ELECTIVE	L	T	P	C
	WIRELESS SECURITY	**3**	**0**	**0**	**3**

AIM:

To understand the security principles of wireless networks.

OBJECTIVE:

- To explore variety of attacks and threats and its impact on MAC layer and Network layer
- To study characteristics, vulnerabilities and challenges of ad hoc networks
- To provide solution for covering the security principles and flaws of popular wireless technologies
- To evaluate the performance of secured routing protocols in MANETs.

Unit I – Attacks on Routing Protocols **9 Hours**

Vulnerability of MANET to attack - review of AODV and DSR - type of attack - active and passive - internal and external - behavior of malicious node - black hole, DoS, Routing table overflow, Impersonation, Energy consumption, Information Disclosure - Misuse type – Misuse goals – Security flaw in AODV -attack on AODV - wormhole and rushing attack -Performance analysis of AODV in the presence of malicious node.

Unit II – Intrusion Detection in Wireless Ad Hoc Networks **9 Hours**

Problem in current IDS techniques - requirements of IDS - classification of IDS – Network and host based - anamoly detection, misuse detection, specification based - intrusion detection in MANETs using distributed IDS and mobile agents - AODV protocol based IDS - Intrusion resistant routing algorithms – Comparison of IDS.

Unit III – Mitigating Techniques for Routing Misbehavior **9 Hours**

Watchdog, Parthrater, Packet leashes and RAP.

Unit IV – Secure Routing Protocols: **9 Hours**

Self organized network layer security in MANETs - mechanism to improve authentication and integrity in AODV using hash chain and digital signatures - on demand secure routing protocol resilent to Byzantine failures - ARIADNE, SEAD, SAR, and ARAN.

Unit V – Challenges in Routing Security **9 Hours**

Security - Challenges and solutions - Providing Robust and Ubiquitous security support - Adaptive security for multilevel Ad Hoc Network - Denial of service Attack at the MAC layer - Detection and handling of MAC layer Misbehavior.

REFERENCES:

1. C.Siva Ram Murthy and B.S.Manoj, *AdHoc Wireless Networks: Architectures and Protocols*, Prentice Hall PTR, 2004.
2. Ivan Stojmenović, *Handbook of Wireless Networks and Mobile Computing*, Wiley, 2002.
3. Hongmei Deng, Wei Li and Dharma P. Agrawal, *Routing Security in Wireless Ad Hoc Networks*, IEEE Communication Magazine, Oct 2002.
4. Peng Ning, Kun Sun, *How To Misuse AODV: A Case Study of Insider Attacks Again Mobile Ad Hoc Routing Protocols* in proceeding of the 4th annaul IEEE information assurance workshop, page 60 – 67 west point, June 2003.
5. Amitabh Mishra, *Intrusion Detection in Wireless Ad Hoc Networks*, IEEE Wireless Communication, February 2004.
6. S.Marti, *Mitigating Routing Misbehaviour in Mobile Ad Hoc Networks*, ACM MOBICOM, 2000.

	ELECTIVE	L	T	P	C
	PATTERN RECOGNITION & ARTIFICIAL INTELLIGENT TECHNIQUES	**3**	**0**	**0**	**3**

AIM:

To gain the knowledge about the procedure for various pattern recognition principles in real world problem.

OBJECTIVE:

- To understand different supervised and unsupervised learning techniques.
- To obtain sound knowledge on recent advancement on pattern recognition techniques.

Unit I – Pattern Classifier **9 Hours**

Overview of pattern recognition - Discriminant functions - Supervised learning - Parametric estimation - Maximum likelihood estimation - Bayesian parameter estimation - Perceptron algorithm - LMSE algorithm - Problems with Bayes approach - Pattern classification by distance functions - Minimum distance pattern classifier.

Unit II – Unsupervised Classification **9 Hours**

Clustering for unsupervised learning and classification - Clustering concept - C-means algorithm – Hierarchical clustering procedures - Graph theoretic approach to pattern clustering - Validity of clustering solutions.

Unit III – Structural Pattern Recognition **9 Hours**

Elements of formal grammars - String generation as pattern description - Recognition of syntactic description - Parsing - Stochastic grammars and applications - Graph based structural representation.

Unit IV – Feature Extraction and Selection **9 Hours**

Entropy minimization - Karhunen - Loeve transformation - Feature selection through functions approximation - Binary feature selection.

Unit V – Recent Advances **9 Hours**

Neural network structures for Pattern Recognition - Neural network based Pattern associators – Unsupervised learning in neural Pattern Recognition - Self organizing networks - Fuzzy logic – Fuzzy pattern classifiers - Pattern classification using Genetic Algorithms.

REFERENCES:

1. 1.Robert J.Schalkoff, *Pattern Recognition: Statistical, Structural and Neural Approaches*, John Wiley &Sons Inc., New York, 2007.
2. Tou and Gonzales, *Pattern Recognition Principles*, Wesley Publication Company, London, 1974.
3. Duda R.O., Hart.P.E., and Strok, *Pattern Classification*, second Edition Wiley, New York, 2008.
4. 4.Morton Nadier and Eric Smith P., *Pattern Recognition Engineering*, John Wiley & Sons, New York, 1993.
5. IEEE Transaction on Pattern Recognition Techniques 2006.
6. IEEE Engineering Medicine and Biology Magazine 2006.

	ELECTIVE	L	T	P	C
	WAVELETS & MULTI-RESOLUTION PROCESSING	**3**	**0**	**0**	**3**

AIM:

To gain the knowledge and skills about various image processing applications.

OBJECTIVE:

- To study the fundamentals of vector and signal spaces.
- To explore the concepts of multi resolution analysis of signals.

Unit I – Introduction **9 Hours**

Vector Spaces - properties - dot product - basis - dimension, orthogonality and orthonormality - relationship between vectors and signals - Signal spaces - concept of Convergence - Hilbert spaces for energy signals - Generalized Fourier Expansion.

Unit II – Multi Resolution Analysis **9 Hours**

Definition of Multi Resolution Analysis (MRA) – Haar basis - Construction of general orthonormal MRAWavelet basis for MRA – Continuous time MRA interpretation for the DTWT – Discrete time MRABasis functions for the DTWT – PRQMF filter banks.

Unit III – Continuous Wavelet Transform **9 Hours**

Wavelet Transform - definition and properties - concept of scale and its relation with frequency - Continuous Wavelet Transform (CWT) - Scaling function and wavelet functions (Daubechies, Coiflet, Mexican Hat, Sinc, Gaussian, Bi-Orthogonal) - Tiling of time -scale plane for CWT.

Unit IV – Discrete Wavelet Transform **9 Hours**

Filter Bank and sub band coding principles - Wavelet Filters - Inverse DWT computation by Filter banks -Basic Properties of Filter coefficients - Choice of wavelet function coefficients - Derivations of Daubechies Wavelets - Mallat's algorithm for DWT – Multi-band Wavelet transforms. Lifting Scheme: Wavelet Transform using Poly phase matrix Factorization - Geometrical foundations of lifting scheme - Lifting scheme in Z –domain.

Unit V – Applications **9 Hours**

Signal Compression – Image Compression techniques: EZW-SPHIT Coding Image denoising techniques- Noise estimation - Shrinkage rules - Shrinkage Functions - Edge detection and object Isolation, Image Fusion, and Object Detection. Curve and Surface Editing-Variation modeling and finite element method using wavelets.

REFERENCES:

1. G,.Strang and T.Nguyen, *Wavelets and Filter Banks*, Wellesley Cambridge Press, 1996
2. M .Vetterli and J.Kovacevic, *Wavelets and Sub-band Coding*, Prentice Hall, 1995
3. S.Mallat., *Wavelet Tour of Signal Processing*, Academic Press, 2008.
4. www.multiresolution.com
5. www.wavelet.org
6. IEEE transactions on Image Processing.
7. IEEE transactions on Neural Networks.

	ELECTIVE	L	T	P	C
	INTRUSION DETECTION & PREVENTION SYSTEMS	**3**	**0**	**0**	**3**

AIM:

To make student understand and recognize the architectures, vulnerabilities and challenges of mobile protocols.

OBJECTIVE:

- To explore basics of intrusion, attacks and detection, prevention techniques
- To study computational systems for intrusion detection systems
- To provide solution for covering the security principles and flaws of popular wireless technologies
- To evaluate the performance of secured routing protocols in MANETs.

Unit I – Introduction **9 Hours**

Understanding Intrusion Detection – Intrusion detection and prevention basics – IDS and IPS analysis schemes, Attacks, Detection approaches –Misuse detection – anomaly detection – specification based detection – hybrid detection.

Unit II – Theoretical foundations of detection **9 Hours**

Taxonomy of anomaly detection system – fuzzy logic – Bayes theory – Artificial Neural networks – Support vector machine – Evolutionary computation – Association rules – Clustering.

Unit III – Architecture and Implementation **9 Hours**

Centralized – Distributed – Cooperative Intrusion Detection – Tiered architecture. Justifying Intrusion Detection: Intrusion detection in security – Threat Briefing – Quantifying risk – Return on Investment (ROI).

Unit IV – Applications and Tools **9 Hours**

Tool Selection and Acquisition Process - Bro Intrusion Detection – Prelude Intrusion Detection - Cisco Security IDS - Snorts Intrusion Detection – NFR security.

Unit V – Legal Issues and Organizations Standards **9 Hours**

Law Enforcement / Criminal Prosecutions – Standard of Due Care – Evidentiary Issues, Organizations and Standardizations.

REFERENCES:

1. Ali A. Ghorbani, Wei Lu, "*Network Intrusion Detection and Prevention:* Concepts and Techniques", Springer, 2010.
2. Carl Enrolf, Eugene Schultz, Jim Mellander, "*Intrusion detection and Prevention",* McGraw Hill, 2004.
3. Paul E. Proctor, "*The Practical Intrusion Detection Handbook* ",Prentice Hall , 2001.
4. Ankit Fadia and Mnu Zacharia, "*Intrusiion Alert",* Vikas Publishing house Pvt., Ltd, 2007.
5. Earl Carter, Jonathan Hogue, "*Intrusion Prevention Fundamentals",* Pearson Education, 2006.

	ELECTIVE	L	T	P	C
	SYSTEM ON CHIP	**3**	**0**	**0**	**3**

AIM:

The students can able to gain knowledge about SoC Design Methodology.

OBJECTIVE:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Unit I

Introduction **9 Hours**

System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.

Unit II **9 Hours**

Design Methodological For Logic Cores

SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores –Designing with hard cores, soft cores- Core and SoC design examples.

Unit III **9 Hours**

Design Methodology for Memory and Analog Cores

Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase- located loops –High I/O.

Unit IV **9 Hours**

Design Validation

Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip

Unit V **9 Hours**

Soc Testing

SoC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories.

Total: 45 Hours

REFERENCES:

1. Rochit Rajsunah, *System-on-a-chip: Design and Test*, Artech House, 2007.
2. Prakash Raslinkar, Peter Paterson & Leena Singh, *System-on-a-chip verification: Methodology and Techniques*, Kluwer Academic Publishers, 2000.
3. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, *Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems*, Springer, 2007.
4. L.Balado, E. Lupon, *Validation and test of systems on chip*, IEEE conference on ASIC/SOC,1999.
5. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, *Integrating BIST techniques for on-line SoC testing*, IEEE Symposium on On-Line testing, 2005.

	ELECTIVE	L	T	P	C
	ELECTROMAGNETIC INTERFERENCE & COMPATIBILITY IN SYSTEM DESIGN	**3**	**0**	**0**	**3**

AIM:

To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

OBJECTIVES:

- To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.
- To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

UNIT I EMI/EMC CONCEPTS **9**

EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES **9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES **9**

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS **9**

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS **9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL HOURS:45

REFERENCES:

1.V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.

2.Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.

3.Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.

4.C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.

5.Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

	ELECTIVE	L	T	P	C
	COGNITIVE RADIO TECHNOLOGY	**3**	**0**	**0**	**3**

AIM:

To gain the ability to identify the various challenges in SDR and CR networks.

OBJECTIVE:

- To explore issues and challenges in SDR and CR networks.
- To understand adaptation of SDR and CR architecture.
- To develop procedure for radio encapsulation and spectrum sensing.

Unit I – Introduction to Software Defined Radio **9 Hours**

Definitions and potential benefits, software radio architecture evolution, technology tradeoffs and architecture implications.

Unit II – SDR Architecture **9 Hours**

Essential functions of the software radio, basic SDR, hardware architecture, Computational processing resources, software architecture, top level component interfaces, interface topologies among plug and play modules,.

Unit III – Introduction to Cognitive Radios **9 Hours**

Marking radio self-aware, cognitive techniques – position awareness, environment awareness in cognitive radios, optimization of radio resources, Artificial Intelligence Techniques.

Unit IV – Cognitive Radio Architecture **9 Hours**

Cognitive Radio – functions, components and design rules, Cognition cycle – orient, plan, decide and act phases, Inference Hierarchy, Architecture maps, Building the Cognitive Radio Architecture on Software defined Radio Architecture.

Unit V – Next Generation Wireless Networks **9 Hours**

The XG Network architecture, spectrum sensing, spectrum management, spectrum mobility, spectrum sharing, upper layer issues, cross – layer design.

REFERENCES

1. Joseph Mitola III,"Software Radio Architecture: Object-Oriented Approaches to Wireless System Engineering", John Wiley & Sons Ltd. 2000.
2. Thomas W.Rondeau, Charles W. Bostain, "Artificial Intelligence in Wireless communication", ARTECH HOUSE .2009.
3. Bruce A. Fette, "Cognitive Radio Technology", Elsevier, 2009.
4. Ian F. Akyildiz, Won – Yeol Lee, Mehmet C. Vuran, Shantidev Mohanty, "Next generation / dynamic spectrum access / cognitive radio wireless networks: A Survey" Elsevier Computer Networks, May 2006.
5. Simon Haykin, "Cognitive Radio: Brain –Empowered Wireless Communications", IEEE Journal on selected areas in communications, Feb 2005.
6. Hasari Celebi, Huseyin Arslan, "Enabling Location and Environment Awareness in Cognitive Radios", Elsevier Computer Communications , Jan 2008.
7. Markus Dillinger, Kambiz Madani, Nancy Alonistioti, "Software Defined Radio", John Wiley, 2003.
8. Huseyin Arslan, "Cognitive Radio, SDR and Adaptive System", Springer, 2007.
9. Alexander M. Wyglinski, Maziarnekovee, Y. Thomas Hu, "Cognitive Radio Communication and Networks", Elsevier, 2010.

	ELECTIVE	L	T	P	C
	NANO ELECTRONICS	**3**	**0**	**0**	**3**

AIM:

This course is offered to students to gain knowledge on Nanoelectronics and various fabrication techniques involved in nanoscience.

OBJECTIVES:

- To Know basic concepts in Nanotechnology.
- To learn the Fundamental of Nano electronics.
- To learn the silicon MOSFET and Quantum Transport Devices.
- To learn the fabrication of Carbon Nanotubes.
- To study about the Molecular Electronics in Nanotechnology.

UNIT I INTRODUCTION TO NANOTECHNOLOGY **9**

Background to nanotechnology: Types of nanotechnology and nanomachines – periodic table – atomic structure – molecules and phases – energy – molecular and atomic size – surface and dimensional space – top down and bottom up; Molecular Nanotechnology: Electron microscope – scanning electron microscope – atomic force microscope – scanning tunnelling microscope – nanomanipulator – nanotweezers – atom manipulation – nano dots – self assembly – dip pen nanolithography. Nanomaterials: preparation– plasma arcing – chemical vapor deposition – sol-gels – electrodeposition – ball milling – applications of nanomaterials;

UNIT II FUNDAMENTALS OF NANOELECTRONICS **9**

Fundamentals of logic devices:- Requirements – dynamic properties – threshold gates; physical limits to computations; concepts of logic devices:- classifications – two terminal devices – field effect devices – coulomb blockade devices – spintronics – quantum cellular automata – quantum computing – DNA computer; performance of information processing systems;- basic binary operations, measure of performance processing capability of biological neurons – performance estimation for the human brain. Ultimate computation:- power dissipation limit – dissipation in reversible computation – the ultimate computer.

UNIT III SILICON MOSFETs& QUANTUM TRANSPORT DEVICES **9**

Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices-scaling rules – silicon-dioxide based gate dielectrics – metal gates – junctions & contacts – advanced MOSFET concepts. Quantum transport devices based on resonant tunneling, Electron tunneling – resonant tunneling diodes – resonant tunneling devices; Single electron devices for logic applications:- Single electron devices – applications of single electron devices to logic circuits.

UNIT IV CARBON NANOTUBES **9**

Carbon Nanotube: Fullerenes - types of nano tubes – formation of nano tubes – assemblies – purification of carbon nanotubes – electronic propertics – synthesis of carbon nanotubes – carbon nanotube interconnects – carbon nanotube FETs – Nanotube for memory applications – prospects of all carbon nanotube nanoelectronics.

UNIT V MOLECULAR ELECTRONICS **9**

Electrodes & contacts – functions – molecular electronic devices – first test systems – simulation and circuit design – fabrication; Future applications: MEMS – robots – random access memory – mass storage devices.

TOTAL HOURS: 45

TEXTBOOKS

1. Michael Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons and BurkhardRaguse, "Nanotechnology: Basic Science and Emerging Technologies", Chapman & Hall / CRC, 2002
2. Rainer Waser (Ed.), "Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices", Wiley-VCH, 20032. T.Pradeep, NANO:"The Essentials–Understanding Nanoscience and Nanotechnology", TMH, 2007

REFERENCES:

1. T.Pradeep, "NANO:The Essentials–Understanding Nanoscience and Nanotechnology", TMH, 2007.

	ELECTIVE	L	T	P	C
	CMOS VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

Analog circuits are essential in interfacing and in building amplifiers and low pass filters. This course introduces design methods for CMOS analog circuit design and implementation of standard MOS integrated circuits and be able to assess their performance taking into account the effects of real circuit parameters.

OBJECTIVE:

At the end of this course the student will be learning, CMOS analog circuits design and simulation using SPICE.

UNIT I - MOS TRANSISTOR THEORY 9

Introduction to I.C Technology. Basic MOS transistors. Threshold Voltage. Body effect. Basic D.C. Equations. Second order effects. MOS models. Small signal A.C characteristics. The complementary CMOS inverter. DC characteristics. Static Load MOS inverters. The differential inverters. Transmission gate.

UNIT II - CMOS PROCESSING TECHNOLOGY 9

Silicon semiconductor technology. Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology. nwell, pwell process. Silicon on insulator. CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latchup.

UNIT III – CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION 9

Resistance estimation. Capacitance estimation. MOS capacitor characteristics.Device capacitances. Diffusion capacitance. SPICE modeling of MOS capacitance. Routing capacitance. Distributed RC effects. Inductance. Switching characteristics. Rise time. Fall time. Delay time. Empirical delay models. Gate delays. CMOS gate transistor sizing. Power dissipation. Scaling of MOS transistor dimensions.

UNIT IV - CMOS CIRCUIT AND LOGIC DESIGN 9

Cmos Logic gate design. Fan in and fan out. Typical CMOS NAND and NOR delays. Transistor sizing. CMOS logic structures. Complementary logic. BICMOS logic. Pseudo nMOS logic. Dynamic CMOS logic. Clocked CMOS logic. Pass transistor logic. CMOS domino logic. NP domino logic. Cascade voltage switch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures.

UNIT V - CMOS SUBSYSTEM DESIGN 9

Data path operations. Addition/subtraction. Parity generators. Comparators. Zero/one detectors. Binary Counters. ALUs. Multiplication. Array, Radix-n, Wallace Tree and Serial Multiplication. Shifters. Memory elements. RWM, Rom, Content Addressable Memory. Control: FSM, PLA Control Implementation.

Total Hours: 45

REFERENCES

1. Neil.H.E. Weste and K.Eshragian, "Principles of CMOS VLSI Design". 2nd Edition. Addison-Wesley , 2000.
2. Douglas a. Pucknell and K.Eshragian., "Basic VLSI Design" 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., "CMOS Circuit Design", 3rd Indian reprint, PHI, 2000.

	ELECTIVE	L	T	P	C
	ANALOG VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

This course is intended to introduce the student to learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

OBJECTIVE:

By the end of the term, students should be able to:

- Demonstrate an understanding of MOS terminal characteristics and capacitive effects.
- Create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGESIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor-Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched -Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks -Floating -Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation -Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter-Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit igma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation -Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test uses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of Statistical Concepts -Statistical Device Modeling-Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 HOURS

REFERENCES:

1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May,"Analog VLSI Design -NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	TESTING OF VLSI CIRCUITS	**3**	**0**	**0**	**3**

AIM:

Testing VLSI is essential as these circuits are complex. Hence this paper deals with fundamental techniques used for logic testing.

OBJECTIVE:

At the end of the course the student will be having knowledge on digital testing as applied to VLSI design.

UNIT I BASICS OF TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

Total Hours: 45

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House,2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

	ELECTIVE	L	T	P	C
	VLSI ARCHITECTURE & DESIGN METHODOLOGIES	**3**	**0**	**0**	**3**

AIM:

This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:

- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

1. INTRODUCTION **9**

Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon's expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

2. ANALOG VLSI AND HIGH SPEED VLSI **9**

Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

3. PROGRAMMABLE ASICS **9**

Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

4. PROGRAMMABLE ASIC DESIGN SOFTWARE **9**

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 - Altera MAX 9000 - Design systems – Logic synthesis – Half gate ASIC – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation

5. LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TOTAL HOURS: 45

REFERENCES:

1. William I. Fletcher “An Engineering approach to Digital Design” Prentice Hall of India 1996
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986
3. M.J.S Smith “Application – specific integrates circuits”, Addison Wesley Longman Inc.1997
4. Frederick J. Hill and Gerald R. Peterson, “Computer Aided Logical Design with emphasison VLSI”.

	ELECTIVE	L	T	P	C
	MOBILE COMPUTING	**3**	**0**	**0**	**3**

AIM:

The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:

At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT – I: WIRELESS TRANSMISSION **9**

Frequency for radio transmission- signals- antennas- signal propagation- multiplexing- modulation- spread spectrum- medium axis control- SDMA- FDMA- TDMA- CDMA- comparisons.

UNIT – II: TELECOMMUNICATION SYSTEM **9**

GSM- DECT- Tetra- UMTS- IMT 2000- GPRS

UNIT – III: WIRELESS LAN **9**

Introduction - Network Taxonomy -IEEE 802.11 standard- hyper LAN - Adhoc network- Bluetooth.

UNIT – IV: MOBILE NETWORK LAYER **9**

Mobile IP- Dynamic post configuration protocol- mobile Adhoc network- DSDV- DSR- AODV- ZRP- OVMR.

UNIT – V: MOBILE TRANSPORT LAYER AND APPLICATION **9**

TCP- WAP- Architecture- WDGP- WTLS- WTP- WSP- WML- WAE- WML script- WTA.

TOTAL HOURS:45

TEXT BOOK

1. Jochen Schiller, "Mobile Communications", Second Edition, Prentice Hall Of India/Pearson Education, 2005.

REFERENCE

1. WILLIAM STALLINGS**, "**Wireless Communications and Networks", Second Edition, Prentice Hall Of India/Pearson Education 2004.

	ELECTIVE	L	T	P	C
	DATA COMMUNICATION AND NETWORKS	**3**	**0**	**0**	**3**

AIM:

To learn all parts of communication software in layered architecture.

OBJECTIVE:

- To study the basics on computer networks and its protocols
- To study the transport layer protocol of OSI model.
- To learn about network layer of OSI model.
- To study data link and MAC layer of OSI model.
- To learn about network security in computer networks.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS 9

An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS 9

Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER 9

Datagram and virtual circuit service - Routing principles - Internet protocols IPVI Addressing and routing datagram format _ IP fragmentation and reassembly - ICMP routing in the internet - Router - Input ports - Switching fabrics - Output ports - Queuing - IPV6 packet format transition from IPV4 to IPV6 Multicast routing.

UNIT IV DATA LINK AND MAC LAYER 9

Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM-X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA 9

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL HOURS: 45

REFERENCE BOOKS:

1. K.Kurose and K.W.Ross - "Computer network" Addison Wesley.(1997)
2. A.S . Tanenbaum "Computer Networks "- (3/e), (2001).
3. T.N.Saadavi,M.H.Ammar & AL . Halleem" Fundamentals of Telecommunication Networks " - Wiley J.K.Buford - "Multimedia Systems" - Addison Wesley.(2001)

	ELECTIVE	L	T	P	C
	DSP PROCESSORS	**3**	**0**	**0**	**3**

AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S **9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP's – Multiple access memory – Multi – port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP's – On Chip Peripherals.

UNIT II: TMS320C5X PROCESSOR **9**

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR **9**

Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV: ADSP PROCESSORS **9**

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS **9**

Architecture of TMS320C54X: Pipe line operation, Code Composer Studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 HOURS

TEXT BOOK:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" - Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008.

REFERENCE BOOKS:

1. User guides Texas Instrumentation, Analog Devices, Motorola.
2. Simon Haykin "Adaptive filter theory", Prentice Hall, 2001.
3. Anil K Jain "Fundamental of Digtal image processing", Prentice Hall, 1989.